IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:	09/778,495	Confirmation No.:	8073
Applicant:	Anderson, et al	Examiner:	Lesniewski, Victor D
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Docket No. : TI-30831

Customer No. : 23494

For: MULTI-PROCESSOR SYSTEM VERIFICATION CIRCUITRY

REPLY BRIEF

Appellant respectfully presents its Reply Brief in response to the Examiner's Answer filed March 12, 2007.

I. Response to Examiner's Argument

A. The combination of DeRoo and Corrigan does not teach the element of a slave processor subsystem as claimed.

1. DeRoo and Corrigan in combination do not show a slave processor, a shared memory accessible by both the master processor and slave processor and an external memory interface allowing slave process to access the system memory.

The Examiner states that the SCP 706 of DeRoo meets the limitation of slave processor, that the common memory 704 of DeRoo meets the limitation of "a shared memory" and that the human user-input interface (HUI) 700 of DeRoo meets the limitation of "an external memory interface allowing said slave processor to access said system memory". The Examiner further states that the HUI 700 allows the SCP 706 to communicate with the CPU (***containing system memory***) in addition to effectuating access of the common memory by both the master processor (CPU) and the slave processor (SCP)" [emphasis added].[1]

The CPU 702, SCP 706, common memory 704 and HUI 700 are shown in Figure 20 of DeRoo. The Examiner provides no citation to DeRoo to support the assertion that the CPU 702 contains system memory, nor has the Applicant determined that the CPU 702 contains system memory. Nonetheless, it is clear from Figure 20 of DeRoo that any memory contained in CPU 702 would be inaccessible to the SCP, since CPU 702 only has *outgoing* address signals (SA[0:17]), without any ports for *incoming* address signals. Therefore, it would not be possible for the SCP 706 to address a memory in CPU 702.

[1] Examiner's Answer, page 11.

Since the HUI 700 cannot pass address signals from the SCP 706 to the CPU 702, the HUI does not meet the limitation of an external memory interface allowing the slave processor to access the system memory.

2. The combination of DeRoo and Corrigan does not show the verification interface.

As noted in Applicant's Appeal Brief, Corrigan shows a shared memory that can be accessed either by (1) a normal path through a primary PCI bus or (2) a loopback path through PCI Bridge (Primary interface) 2, pad flow circuit 6, pad 8, pad flow circuit 6 (a second time), shared memory bridge 4, and shared memory bus 250. Thus, whether the Corrigan device is in normal mode or loopback mode, the same memory is being accessed – the only difference is that a different path is taken to get to that memory.[2] Corrigan thus teaches the use of *two paths* to the *same* memory; it does not show a verification interface that can pass system memory access to either one of *two memories* responsive to a signal.

The Examiner states, however, that the verification circuit is shown because "the combination would teach a CPU with a system memory on the second bus as DeRoo clearly teaches communications between the SCP and CPU…". First, as explained above, DeRoo does not teach a system memory on a CPU that can be accessed by the SCP – it is clear that no such memory exists. Accordingly, there would be no path between the SCP and the CPU of DeRoo which could be modified by the teachings of

[2] Appeal Brief, page 16, second full paragraph through page 18, first paragraph.

Corrigan. Second, Corrigan does not show an interface that switches between memories responsive to a signal; thus, there would be no reason to use it to accomplish the function provided by the verification circuit of the present claims.

3. The combination of DeRoo and Corrigan does not show circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device or a verification mode for testing the processing device, where the verification circuitry passes memory accesses to a system memory or a shared memory responsive to the signal.

The Examiner states that the ISOLATE signal of DeRoo can effectuate a test mode. This is simply not true – the ISOLATE signal is used *during* a test mode to place the output pins in a high impedance state.[3] The ISOLATE signal is not and cannot be used to *initiate* a test mode, since it is also used during non-test mode functions such as battery charging. It could not be used in the present invention to control the verification circuitry – that would mean that every time a non-test function, such as battery charging, was active, the device would begin to pass memory accesses meant for the system memory to the shared memory.

[3] DeRoo, colum 19, lines 36-38.

II. Conclusion

The limitations discussed above are present in all of the independent claims 1, 8 and 13. For these reasons, Appellant submits that all of the claims on appeal in this case are both novel and non-obvious over the prior art of record in this case. Appellant therefore respectfully submits that the final rejection of claims 1 – 20 is in error. Reversal of the final rejection of the claims in this case is therefore respectfully requested.

Respectfully submitted,

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